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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,812	11/18/2003	Jong-Hoon Oh	2003P52888US	5194

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EXAMINER	
LE, THONG QUOC	
ART UNIT	**PAPER NUMBER**
2827	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,812	OH, JONG-HOON	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-15,17 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11, 13, 20-27* is/are rejected.

7)☒ Claim(s) *12,14,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 05/07/2007 has been entered.

2. Claims 11-15, 17, 20-27 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 11-15, 17, 20-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 11, 13, 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Woo et al. (Pub. U.S. Patent No. 2003/002811).

Regarding claim 11, Woo et al. disclose a method for selectively refreshing rows of memory cells in one or more semiconductor memory devices (Figure 1) , comprising:

monitoring, by a memory controller (Figure 2, 14) coupled with the semiconductor memory devices (Figure 2, 16) , write operations to the memory cells;

maintaining a plurality of bits indicative of rows (Figure 1, 24, [0024], each bit or flag is set to indicate whether the corresponding row is actually un use and whether it therefore needs to be refreshed) containing memory cells involved in the monitored write operations on the memory controller ([0024]);

transferring a first plurality of the bits to a first memory device ([0025], Figure 3); and

placing the first memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the first plurality of bits ([0027], Figure 5, 34, [0043-0046).

Regarding claim 13, Woo et al. disclose a semiconductor memory device (Figure 1), comprising:

a plurality of rows of memory cells (Figure 2, 22);

refresh circuitry (Figure 1, 21) configured to issue refresh requests for the rows of memory cells when the memory device is placed in a self-refresh mode;

row state circuitry(Figure 1, 24) configured to maintain a plurality of bits indicative of rows that are to be refreshed;

pins configured to receive the plurality of bits from a memory controller and to transfer the plurality of bits to the row state circuitry ([0024-0025]); and

refresh enable circuitry (Figure 1, 12) configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry.

Regarding claim 24, Woo et al. disclose wherein the plurality of bits is indicative of rows that have been written to and are to be refreshed ([0024]).

Regarding claim 25-26, Woo et al. disclose issuing a self-refresh command from the memory controller to the memory device (Figure 1).

6. Claims 20-23, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Shi et al. (Pub. U.S. Patent No. 2005/0002253).

Regarding claim 20, Shi et al. disclose a system (Figure 1), comprising:

a memory device (Figure 1, 110) having a plurality of rows of memory cells (Figure 1, row0-row X), wherein the memory device is configured to limit the number of rows that are refreshed ([0017], refresh operations to refresh rows of memory cells), during a self-refresh mode, based on row data indicative of rows that are to be refreshed ([0002], [0019]); and

a memory controller (Figure 2, 240) configured to monitor write operations (Figure 3, [0031], monitoring software) to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self-refresh mode (Figure 3, [0030-0031], Figure 5).

Regarding claim 21, Shi et al. disclose wherein: the row data is stored in the memory device in an array of memory cells (Figure 1, 110); and the memory controller is further configured to reset the array of memory cells prior to transferring the row data to the memory device ([0044]).

Regarding claim 22, Shi et al. disclose wherein the memory controller is configured to reset the array of memory cells by writing to a mode register of the memory device ([0024]).

Regarding claim 23, Shi et al. disclose wherein the memory controller (Figure 2, 240) is configured to set a bit in the row data to indicate one or more cells in a corresponding row have been written.

Regarding claim 27, Shi et al. disclose wherein the memory controller is configured to issue a self-refresh command to the memory device (Figure 5, 510, [0033]).

Allowable Subject Matter

7. Claims 12, 14-15, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12, 14-15, 17 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Shi et al. (Pub. U.S. Patent No. 2005/0002253), Woo et al. (Pub. U.S. Patent No. 2003/0028711), and others, does not teach the claimed invention

having transferring a second plurality of the bits to a second memory device; and placing the second memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the second plurality of bits, and wherein the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued by generating a signal used to inhibit refresh requests.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827